ECE3663 Digital Integrated Circuits

Design Review 1

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So far for our design project we have completed all of the tasks for design review 1.  These include the design of the following components: a 16 bit AND gate, a 16 bit NOR gate, a 16 bit PASS gate, and a 1 bit 8:1 mux.  These were all created via schematic rather than netlist, since it was simpler to make wire carry 16 bits that way than to figure out how to implement that in a netlist.  When we extracted the netlists for simulation, this proved to be a good decision because the netlists were very long (because of all the bits) and it would have been easy to make a mistake (and difficult to find).  Additionally we successfully simulated all of the circuits using those netlists in Ocean to show that they functioned the way they should.  The schematics and simulation results are attached.

The final part of the design review was to create a block diagram of the ALU we would be constructing.  This is attached as well and was fairly simple to design.  In essence, the mux can be used to select which function you wish to implement (AND,OR, PASS, etc).  The arbitrary function we are thinking about implementing is XNOR. XNOR is a functionally complete operation with many uses,especially when dealing with signed integers.  After the design review is completed we will revise it based on feedback and suggestions.

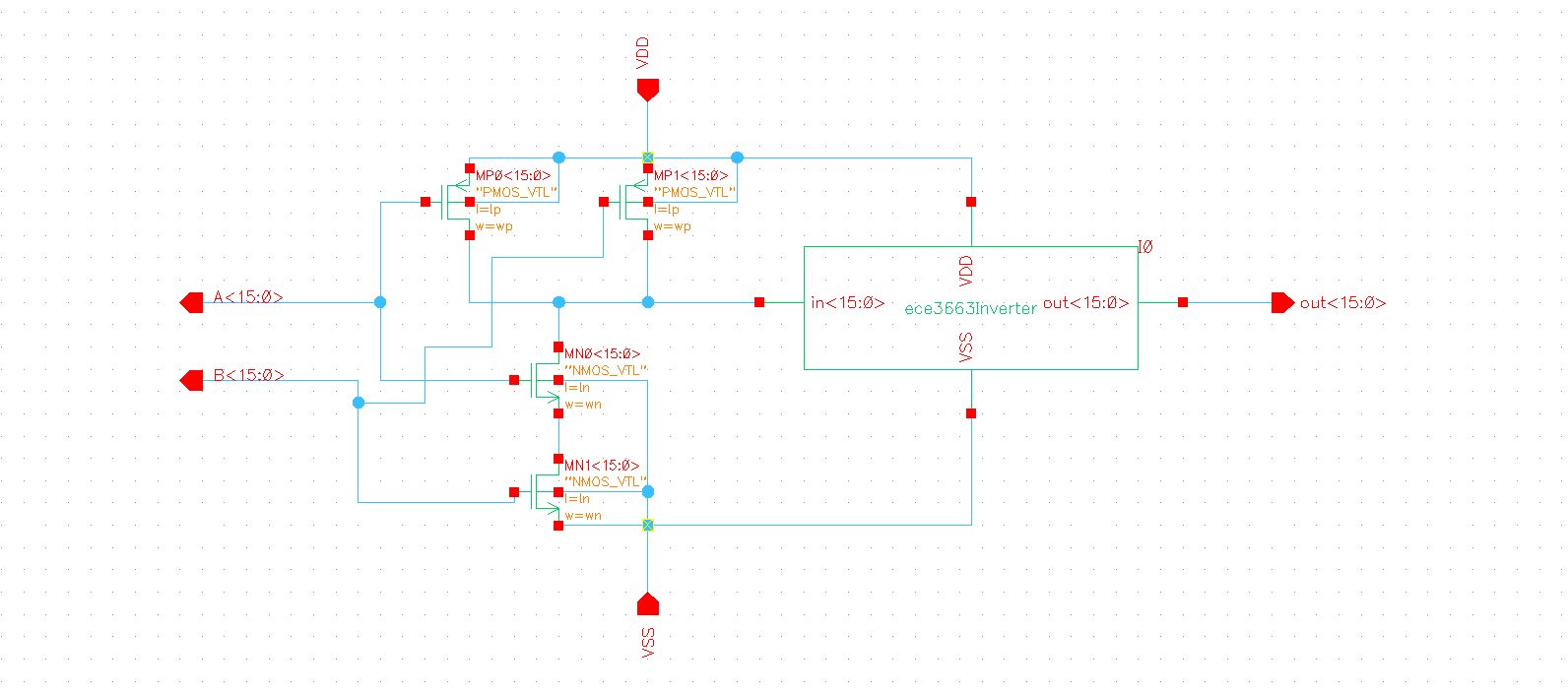
For the next design review, we will have to have completed the following ALU functions: ADD,SHIFT, and SUB.  Furthermore, we should have the ALU connectivity correctly working with the completed functions as well as registers which must also be designed.  To verify working condition, an appropriate amount of Ocean simulation will be done.  We anticipate constructing these circuits in schematic form as well.

After the receiving feedback from the second design review and revising it, we must complete the ALU by adding the function NOP and our arbitrary function (possibly XNOR).  Complete functionality will be well tested and metrics such as delay and power will be measured.  Finally, a report and presentation will be delivered.

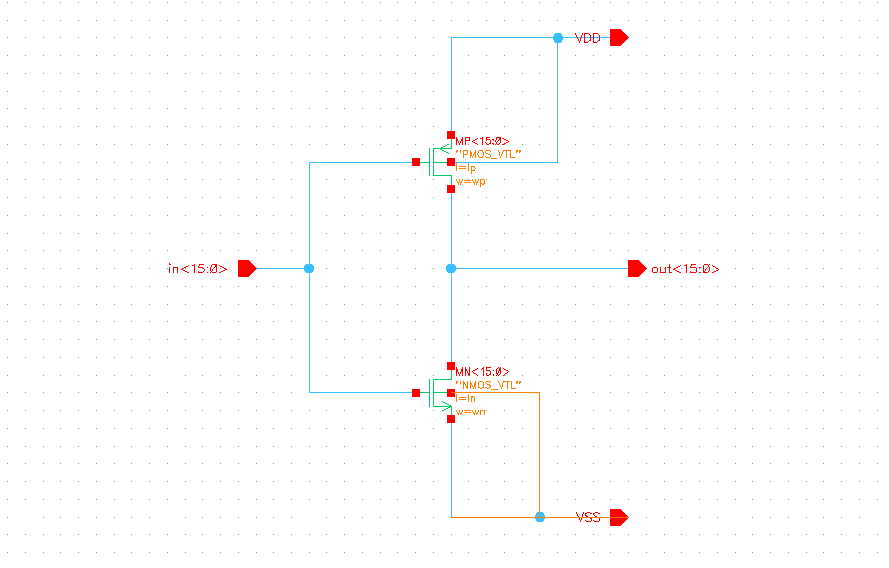
Throughout this whole process we will be keeping in mind the desired metrics which are delay (most important)  and area and power (of equal importance).  We will also be updating our wiki page with progress and results.

Schematics:

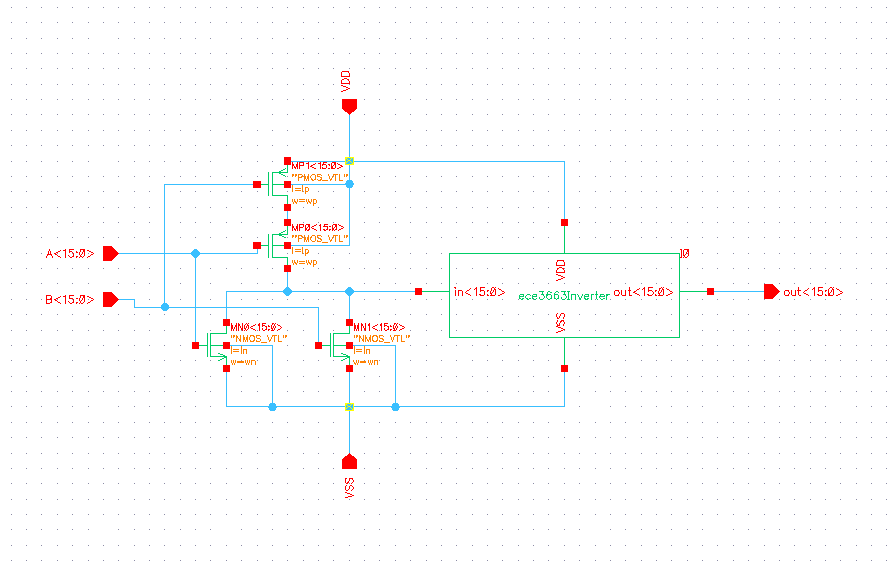
16bit AND (uses 16bit inverter)



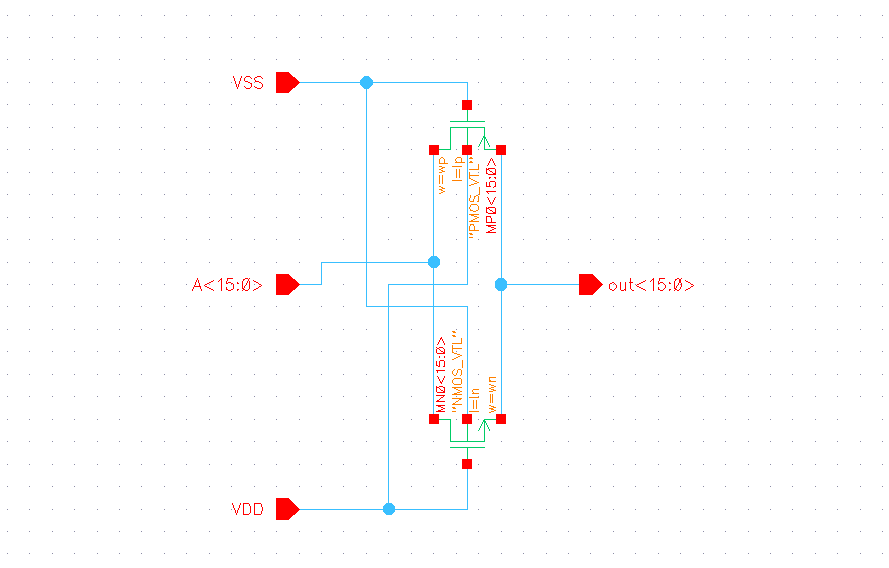
16bit Inverter



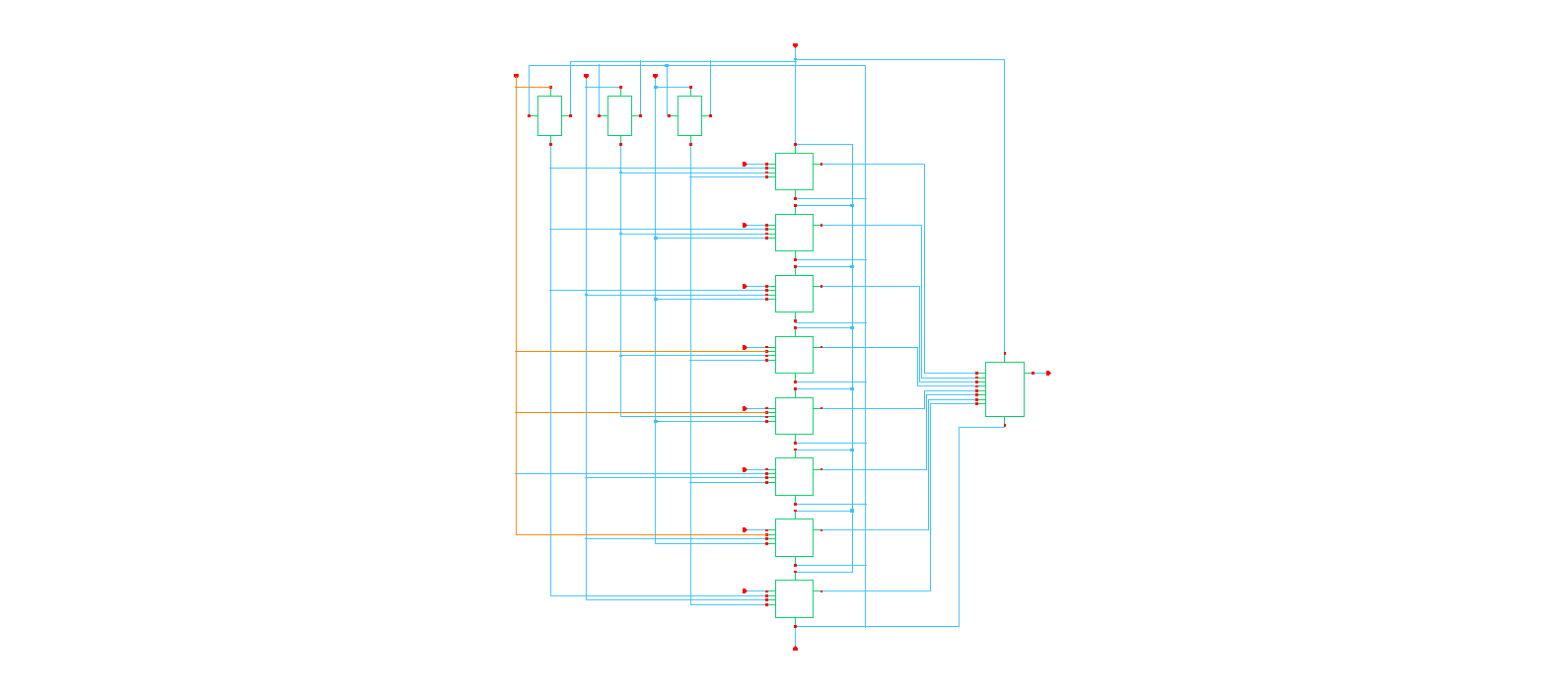
16bit OR (uses same 16bit Inverter)



16bit PASS



1bit 8 to 1 Mux (uses 4bit AND, 4bit OR, 1bit Inverter)



1b Inverter

VDD

Inputs

Select lines

4bit AND

4bit OR

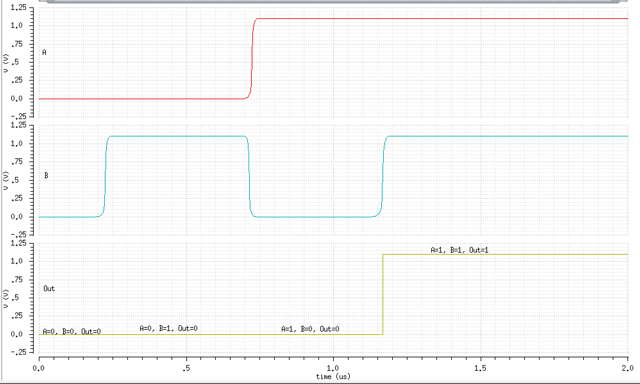
VSS

The schematics for the 4bit AND, 4bit OR, and 1b Inverter look exactly the same as their 16b counterparts except the bits on the line correspond to their bit number

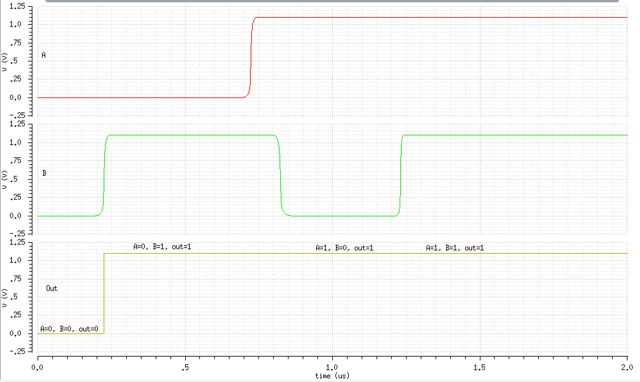
Simulations to test for functionality

: All schematics were converted into netlists and simulated with Ocean. Two inverters buffered each input and a load of the same circuit being tested was used but with a fannout of 4. This provided a load of 4 times the width of the circuit.

16bit AND



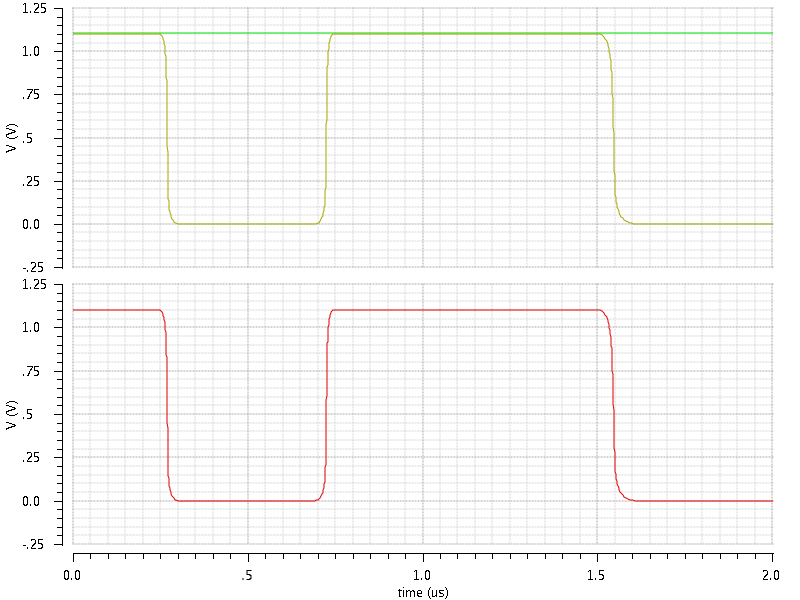
In the plot the red line represent the A input and the blue line represents the B input. The last line is the response. As it can be seen, it follows the logic of and AND gate and it pulls all the way up and down.

16bit OR

As before, the top plot is A, the middle B, and the bottom the output. As it can be seen the logic follows that of an OR gate and the voltages pull all the way up and down.

PASS

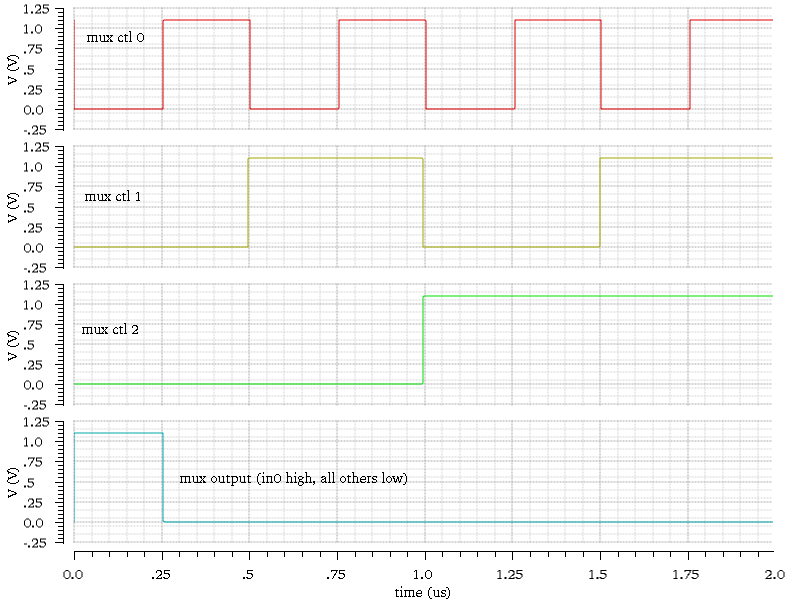
VDD

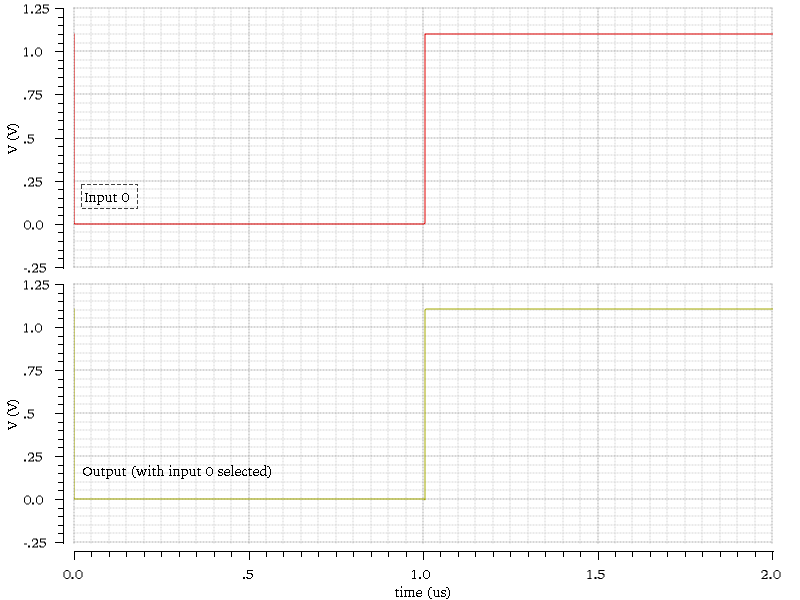


In

OUT

This is the plot for the PASS gate when the gate of the Nmos is 1 and the gate of the Pmos is 0. The top plot is the output and vdd for comparison. The bottom plot is the input. As it can be seen, the signal is passed through exactly as it goes in.

1bit 8:1 Mux

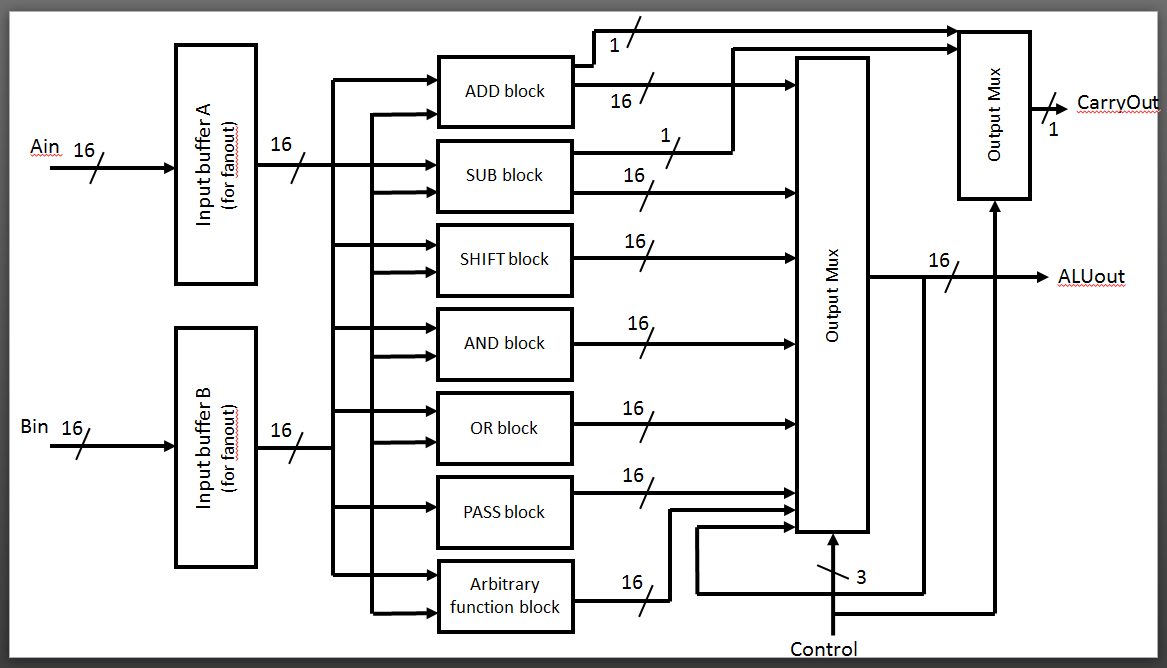


In the first image, the first three plots represent the control lines and the 4th is the output when the input0 is equal to vdd and all other inputs are equal to vss. The control lines cycle through all posibilitites and show that input0 is only passed through when the three selects are at 0.

The second image shows the mux selecting input0 and how the output changes to equal the value of input0.

Together these images show the functionality of the 1b 8:1 mux

Finally, here is the block diagram of the ALU we are designing:



The two 16b inputs are applied to the different logic blocks on a clock cycle. The logic is performed and sent to the 8:1 mux where the select lines determine the output based on the logic that was desired. For the cases of the ADD and SUB where there can be a carryout (from adding or 2’s complement) a carry out is also outputted if the ADD or SUB were selected. This output would then go to a register where it is also stored or passed through on a clock cycle.